CLAIMS

What is claimed is:

1. A packaging method of a package for electronic elements, comprising the steps of:

a) providing a substrate;

b) forming a plurality of stud bumps on a supporting surface of the substrate by a stud bump process;

c) providing at least one electronic element having a plurality of vias, wherein the stud bumps are arranged in a manner to respectively correspondingly pass through the vias; and

d) aligning the stud bumps with the vias and passing the stud bumps respectively through the vias to securely mount the electronic element on the substrate.

2. The method of claim 1, further comprising a step of stacking additional electronic elements on one another according to the steps a) to d).

3. The method of claim 1, further comprising the steps of applying a solder paste over the stud bumps on an exposed surface of the topmost electronic element, and reflowing the solder paste to allow the solder paste to flow down through the vias along the stud bumps so as to securely connect the electronic elements.

4. The method of claim 1, further comprising the steps of applying a liquid conductive glue over the stud bumps on an exposed surface of the topmost electronic element and allowing the conductive glue to flow down through the vias along the stud bumps so as to securely connect the electronic elements.

5. The method of claim 1, wherein the material of the stud bumps is a conductive metal.

6. The method of claim 1, wherein the material of the stud bumps is gold, copper or aluminum.

7. The method of claim 1, wherein the electronic element is a silicon chip, GaAs chip, InP chip or epitaxily-grown chip.

8. The method of claim 1, wherein the substrate is an organic substrate, a ceramic substrate, a glass substrate, a silicon substrate or a GaAs substrate.

9. A stacked package for electronic elements, comprising:

a substrate, having a supporting surface, wherein a plurality of stud bumps are formed on the supporting surface by a stud bump process; and

an electronic element, having a plurality of vias corresponding to the stud bumps, wherein the vias are respectively aligned with the stud bumps to securely mount the electronic element on the substrate.

10. The stacked package for electronic elements of claim 9, wherein the material of the stud bumps is a conductive metal.

11. The stacked package for electronic elements of claim 9, wherein the material of the stud bumps is gold, copper or aluminum.

12. The stacked package for electronic elements of claim 9, wherein the element is a silicon chip, a GaAs chip, an InP chip or an epitaxily-grown chip.

13. The stacked package for electronic elements of claim 9, wherein the substrate is an organic substrate, a ceramic substrate, a glass substrate, a silicon substrate or a GaAs substrate.

14. A stacked package for electronic elements, comprising:

a substrate, having a supporting surface, wherein a plurality of stud bumps are formed

on the supporting surface by a stud bump process; and

a plurality of electronic elements, each having a plurality of vias corresponding to the stud bumps, wherein the vias of each electronic element are respectively aligned with the stud bumps, the stud bumps being allowed to pass through the vias so as to securely mount and stack the electronic elements on the substrate.

15. The stacked package for electronic elements of claim 14, further comprising a solder paste that is applied over exposed surfaces of the stud bumps on the topmost electronic element, the solder paste being reflowed to flow down through the vias along the stud bumps so as to securely connect the electronic elements.

16. The stacked package for electronic elements of claim 14, further comprising a conductive glue that is applied over the stud bumps on an exposed surface of the topmost electronic element, and flows through the vias along the stud bumps so as to securely connect the electronic elements.

17. The stacked package for electronic elements of claim 14, further comprising a spacer between adjacent electronic elements.

18. The stacked package for electronic elements of claim 14, wherein the material of the stud bumps is a conductive metal.

19. The stacked package for electronic elements of claim 14, wherein the material of the stud bumps is gold, copper or aluminum.

20. The stacked package for electronic elements of claim 14, wherein the element is a silicon chip, a GaAs chip, an InP chip or a epitaxily-grown chip.

21. The stacked package for electronic elements of claim 14, wherein the substrate is an organic substrate, a ceramic substrate, a glass substrate, a silicon substrate or a GaAs substrate.